**(Clean Version of Specification Amendments)**

Title:

DFT RESULT DIAGNOSIS SYSTEM AND METHOD

Page 1, lines 5 - 7:

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The invention relates generally to automatic test equipment and more particularly a DFT result diagnosis system and method for designing, testing and diagnosing semiconductor devices.

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However, as device complexities and densities increase, the cost of the conventional functional test approach can increase dramatically. In particular, the volume of functional test pattern data required to achieve acceptable fault coverage may increase exponentially with the size of the device. To offset these costs, many semiconductor manufacturers have looked towards structured design-for-testability (DFT) methods. With structured DFT methods the goal changes from verification of functionality to finding manufacturing defects. These methods generally rely on additional circuitry provided on the device to enhance the controllability and observability of the internal state of the device. Examples of DFT methods include scan testing, built-in-self-test (BIST), and core test (embedded microprocessor cores, etc.).

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While the conventional techniques described above are beneficial for their intended purposes, the lack of automation between the ATE and the diagnosis tool is problematic. Existing pattern conversion tools are not integrated with the result translation process, so existing result translation solutions generally embed knowledge about the particular ATPG/diagnosis tool, pattern conversion tool, ATE, test program, and/or device and must therefore be modified when any of these changes. Moreover, the failure data identified and processed is typically not readily user-comprehensible. The DFT result diagnosis system and method of the present invention addresses these problems.

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The DFT result diagnosis system and method of the present invention provides a unique automated and visual approach to testing semiconductor devices with ATE and DFT tools. This minimizes diagnosis time for devices-under-test, thereby optimizing the design-to-production timetable for semiconductor devices.

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To realize the foregoing advantages, the invention in one form comprises a DFT result diagnosis system. The system includes an ATE data source for providing test data in the ATE domain. An ATPG tool is operative to generate ATPG pattern data and ATPG results data in the ATPG domain. At least one translation module is provided to automatically convert data between multiple domains. Additionally, the system includes at least one function module to automatically summarize data from one or more devices or tests in one or more domains.

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In a further form, the invention comprises a method including the steps of capturing scan failure data associated with failed scan chains from a data source; displaying a portion of the scan chains including the captured failure data; and diagnosing the scan failure data with a diagnosis tool to produce diagnosis results data.

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FIG. 1 is a simplified block diagram of a DFT result diagnosis system according to one form of the present invention;

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Electronic design automation (EDA) software gives semiconductor device manufacturers a tool for troubleshooting and refining their circuit designs before entering mass production. Employing EDA tools with production-oriented ATE provides real-world test solutions not only for the pre-production stage, but also in post-production where new failures may materialize that might be indetectable through simulation alone. The present invention seamlessly integrates EDA software with the ATE software to create a DFT result diagnosis system, generally designated 20 (Figure 1), to fully automate the process.

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Referring to Figure 1, the DFT result diagnosis system 20, in one form comprises a scan diagnosis system that employs a test and diagnosis engine 30 that couples to a device-under-test (DUT) 22. A graphical-user-interface (GUI) 60 ties-in to the test and diagnosis engine to provide real-time visual monitoring of the various functions provided by the present invention, more fully described below.

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Further referring to Figure 1, respective pattern, test and diagnosis results translator modules 40, 50 and 70 convert data used by the ATE 32 and the EDA tool 34 to provide an automatic and seamless integration between the software packages. The pattern translator module 40 performs ATPG to ATE vector conversion, and generates test patterns which may be compiled and loaded onto the ATE. The pattern translator module also includes a map generation component 42 which generates a pattern map (shown as direct data at 43) between ATE and ATPG pattern domains and also captures information describing the locations of scan load/unload sequences within the ATE/ATPG patterns.

Use of the term "domain" herein, consistent with that understood in the art, is intended to convey a type of data. For example, data in the ATE test result domain might include failing ATE patterns, failing pins, and/or failing cycles. Data in the ATPG test results domain might include failing ATPG patterns, failing ATPG pins, and so forth. Likewise, failures of DFT test structures (such as scan chains or cells), failures of logical design elements (such as gates), and failures at physical design locations also have their respective domains.

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Referring now to Figure 2, the test result translator module 50, in further detail, includes a first converter T1, which takes the ATE-specific ASCII output data from a datalog source, such as for example the tester 32, or some other data repository, (essentially a list of failing vectors in the ATE domain indicating the failing ATE patterns, addresses, cycles, and device pins), and converts it into a general datalog format in the ATPG domain (referencing ATPG pattern names). The general datalog format combines elements of both the ATE and ATPG data formats. Additionally, correlation data from the mapping generator also feeds into the converter T1 to associate scan chain location data with the vector pattern data.

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A series of functions are operable on the general datalog through the function module A1, such as filtering, sorting, accumulating and querying of data. The results of these functions, or summarizations, are viewable by a user through optional selection menus in the GUI 60. Filtering and sorting may involve looking at some part of the data, while excluding other portions, or subsets of the data. The accumulating function, as illustrated in Figures 7 and 8, gives the user the ability to look at various aspects of the data, across multiple tests (if desired) in an effort to gain a better understanding of the result interpretation. For example, a user could accumulate data across multiple tests on a device, or accumulate data from multiple devices to identify which pins, tests, scan chains, scan cells, logical design elements, and/or physical design elements are failing most frequently.

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The general datalog is then converted by a second converter T2, into a general datalog domain that includes ATPG information. This data is is optionally processed through function module A2, and subject to filtering, accumulating, etc. A third conversion is performed by converter T3, where the general datalog ATPG data is transformed into scan-cell failure domain data, indicating ATPG pattern names, scan chain names, and scan cell numbers. Like the general datalog data, the general scan cell failure data is subject to processing through function module A3 (filtering, sorting, accumulating, querying) as desired. A fourth converter T4, then takes the general scan cell failure data and transforms it into a format suitable for the specific diagnosis tool employed.

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The diagnosis result translator 70, shown in Figure 3, feeds ATPG specific data from the diagnosis engine 38, through converter T5 to produce general diagnosis results. Function module A5 provides optional data processing functions, as desired, such as filtering, accumulating, and the like.

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As noted above, processing through the test and diagnosis engine 30 is conveniently monitored by a user through menu selections on the GUI 60. The GUI includes several interactive screens (Figures 6 through 8) that present a user with an array of options to visualize data in any number of formats for optimal diagnosis of the data. This provides a user with maximum flexibility in determining and diagnosing problem areas in a DUT design, and can be used to reduce the volume of data which must be processed by the next step, thus reducing turnaround time. Of particular significance is the ability of the GUI to actually show sequences of scan chains for rapid evaluation by the user. This is more fully described below.

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Initially, at step 100, the diagnosis tool 34 generates ATPG test patterns designed to serially shift along the scan chains (flip-flops disposed within the DUT 22) to determine failures in areas of the device not normally accessible by conventional ATE patterns. In order to get the patterns into the device, however, they must first be translated into the appropriate ATE vector format. As noted above, this is automatically carried out by the pattern translator 40, at step 102. The ATE 32 then processes the vector data to test the DUT, at step 104, resulting in the capture of scan failure data, at step 106. The captured data is then converted and processed by converter T1 and function module A1 (Figure 2), at step 108, to produce general ATE datalog data.

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From this point, the user then directs the translation of the ATE datalog output data into the general ATPG datalog format with converter T2 and function module A2, at step 112. The general ATPG datalog data may then be displayed, at step 114.

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With the data fully converted, the diagnosis tool may then be directed, at step 122, to diagnose the scan failures. Following a fifth data conversion by the diagnosis results translator 70, with T5, at step 124, the results of the diagnosis may then be viewed by a user as logical defect data, at step 126. Figures 5 and 6 illustrate screens showing available options and results associated with these steps as reflected in the GUI 60.

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After diagnosis processing, the data may be further diagnosed or processed, as desired by the user. In some instances, the user may want to view a physical design map for the device to further understand the defects diagnosed. This may be accomplished through the use of additional software, such as that available from Knights Technologies, and known under the trademark "LogicMap" TM.

Page 9, lines 12 - 20:

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Those skilled in the art will appreciate the many benefits and advantages afforded by the present invention. Of significant importance is the automation capability provided by the translator modules, which serve to seamlessly convert data between the respective ATE and EDA tool domains, and the function modules, which provide automatic diagnoses of the data. This eliminates the need for costly and untimely batch processing to process data from one format to another. Further, by providing a flexible GUI that monitors all phases of the test and diagnosis, including visually illustrating failing scan chain sequences, an understanding of the failures involved may be more easily comprehended and diagnosed by the semiconductor device manufacturer.

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While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention. For example, while the discussion herein is couched in terms specific to scan-based DFT methodologies, the diagnostic aspect of the invention also applies to BIST and core-test DFT methods.